Conversion

Lecture 15

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Conversion:

In general, most of the information is analog in nature, where a digital quantity can have only discrete values which are expressed in a digital code. There are three steps as –

Conversion analog input into digital form

Processing the digital information

Conversion the digital output to analog form

$$Physical\ Variable \rightarrow Measuring\ Device \rightarrow ADC \rightarrow Digital\ Processing \rightarrow DAC \rightarrow Controller\ of\ Physical\ Variable$$

Digital to Analog Conversion(DAC):

It is the process of converting a value in digital code in binary coded decimal system (BCD) into a voltage or current proportional to digital value. . It is also called decoding device.

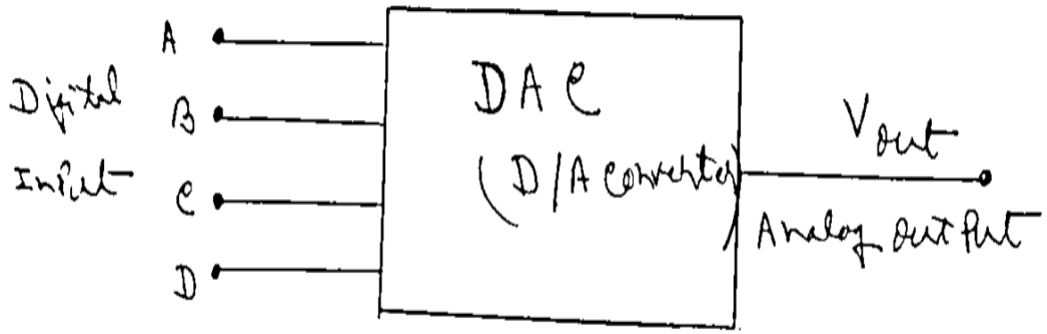

Fig 1

Here A, B, C, D are digital inputs of either 0 or 1. There are $2^4 = 16$ possible combinations of inputs. For each input like 0000, 0001, …..,1111, the DAC gives a unique value of voltage or current as output.

$$The\ analog\ output \propto Digital\ input$$
$$Analog\ output = K \times Digital\ input$$

Where K is constant of proportionality and is constant for a given DAC.

Actually the output of a DAC is not a true analog quantity, because it can take only specific values. But by increasing the number the input bits, the number of possible output values can be increased and the step size which is the difference between two successive output values can be reduced.

Then the output will be more closer to the analog quantity. The following *figure 2* shows the output form of a DAC.

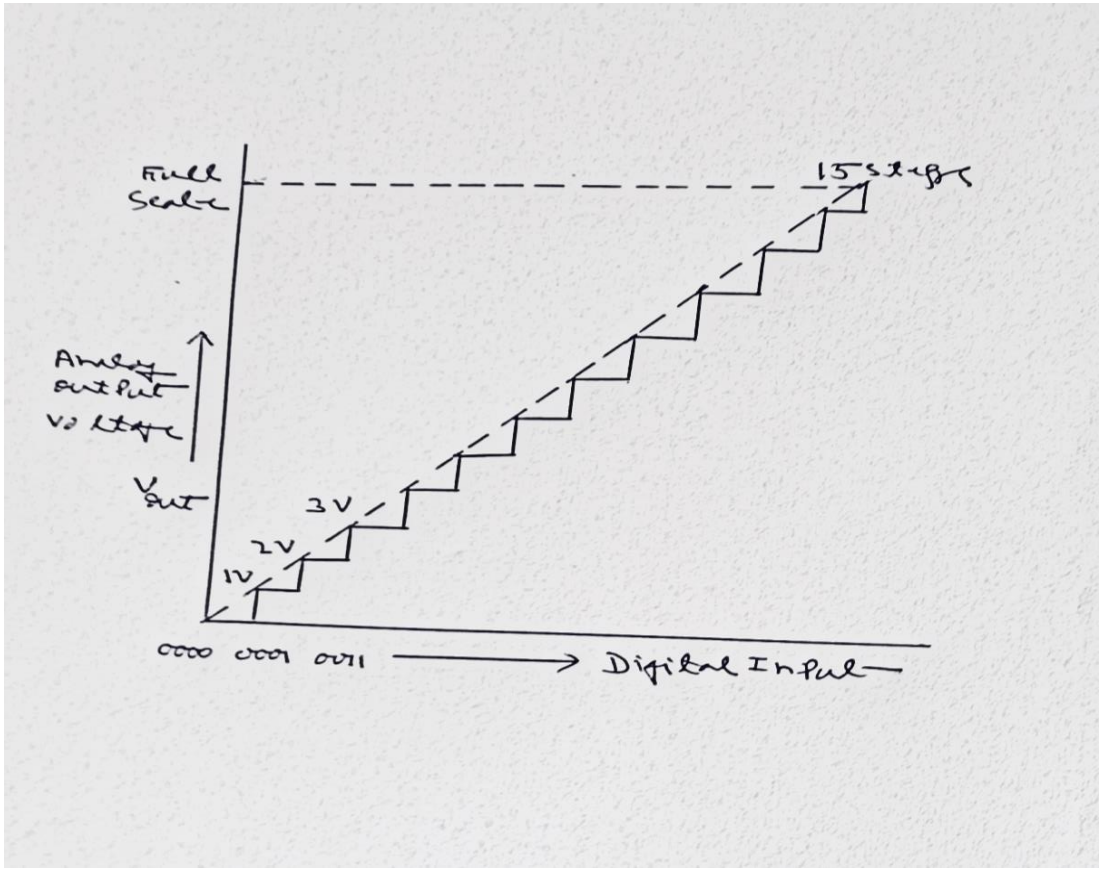

Fig 2

Parameter of DAC:

Resolution

The resolution or step size of a DA converter is defined as the smallest change that occurs in an analog output due to change in the digital input.

The resolution of a DAC is also defined as the reciprocal of the number of discrete steps in the full output of DAC. It is also the size of jumps in the staircase wave form. The step size is the change in V_{out} as the digital input value is changed from one value to the next.

For *n-bit* DAC, the number of different levels will be 2^n and hence number of steps will be $2^n - 1$.

Thus

$$Percentage\ of\ resolution = \frac{1}{2^n - 1} \times 100\%$$

The greater the number of bits, more will be number of steps and smaller will be the steps size and the system is said to have better resolution. But with more number of input bits the DAC becomes more expensive.

Accuracy

The accuracy of DAC is defined in terms of full scale error and linearity error. Full scale error of a DAC is maximum deviation of the output value of DAC from the ideal output value expressed as a percentage of full scale. The linearity error is the maximum deviation of the analog output from the ideal output.

Binary Ladder or R-2R Ladder DAC:

This type of DAC uses a ladder network of series parallel combination of two resistors of vales of R and 2R. The following figure shows the R-2R ladder DAC having 4-bit digital input.

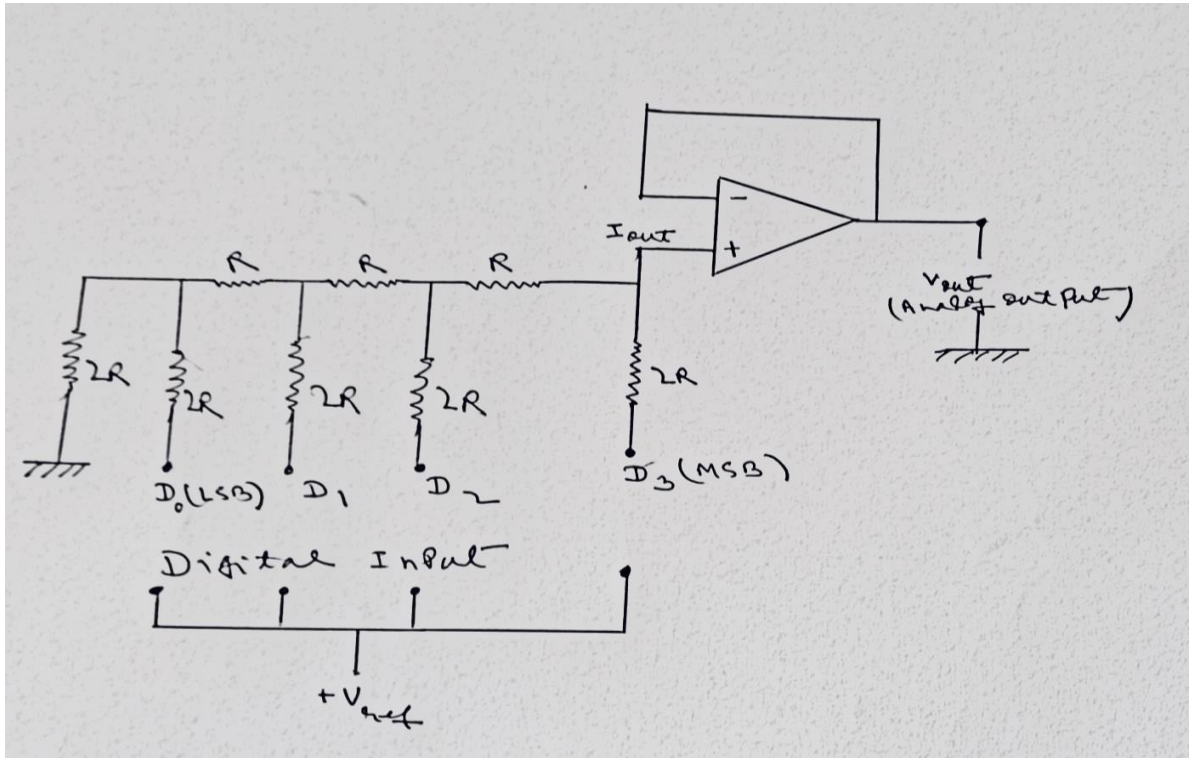

Fig 3

The output current I_{out} depends on the digital inputs $D_0, D_1, D_2\ and\ D_3$. This current then flows through an OPAMP that acts as current to voltage converter and to give V_{out} .

The analog output voltage V_{out} is proportional to the digital input given by the

$$V_{out} = \frac{D_0 \times 2^0 + D_1 \times 2^1 + D_2 \times 2^2 + D_3 \times 2^3}{2^4} V_{ref}$$

In general

$$V_{out} = \frac{D_0 \times 2^0 + D_1 \times 2^1 + \cdots + D_{n-1} \times 2^{n-1}}{2^n} V_{ref}$$

It means for more digital inputs, more steps will be there using more sections of ladder network and better will be resolution.

But cost of DAC will be increase. Voltage resolution for n-stage ladder network will be $\frac{V_{ref}}{2^n}$.

Weighted-Resistor DAC:

In weighted-Resistor type DAC, the OPAMP is used to produce a weighted sum of the digital inputs in which the weights are proportional to the weights of the bit positions of inputs.

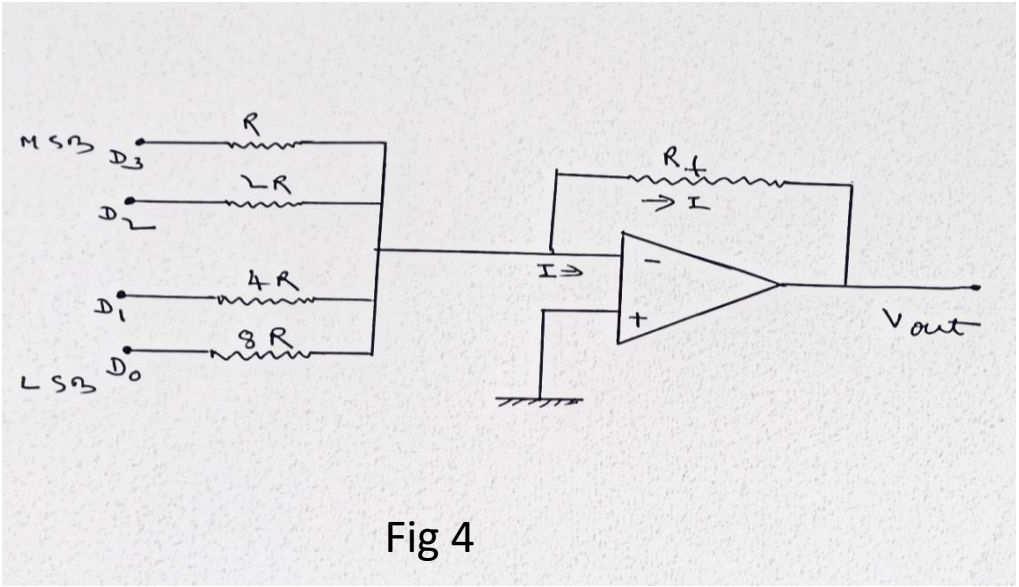

Fig 4

In this DAC , OPAMP is connected as an inverting amplifier and hence each input is amplified by a factor equal to the ratio of the feedback resistance divided by the resistance to which it is connected as shown in figure . The most significant bit (MSB) D_3amplified by $\frac{R_f}{R}$, D_2 is amplified by $\frac{R_f}{2R}$, D_1 is amplified by $\frac{R_f}{4R}$ and D_0, the least significant bit (LSB) is amplified by $\frac{R_f}{8R}$.

The inverting terminal of the OPAMP acts as a virtual ground. Since the OPAMP adds and inverse

$$V_{out} = -\left(D_3 + \frac{D_2}{2} + \frac{D_1}{4} + \frac{D_0}{8}\right) \times \frac{R_f}{R}$$

The disadvantage of this type of DAC is that a different valued precision resistor has to be used for each bit position of the digital input and there will be a large difference in resistor values required for LSB and MSB. It is also important that resistor for MSB should be able to handle larger current than that of LSB.

Analog to Digital Converter (ADC):

In this converter $V_{in}\ and\ V_{ref}$ are the analog input voltage and reference voltage where D_{out} is the n-bit digital output. Therefore analog to digital converter (ADC) produces a digital output that a proportional to the value of input analog system.

For ADC converter signals are represented as

$$V_{ref}\left(D_0 2^{-n} + D_1 2^{-(n-1)} \ldots . + D_{n-1} 2^{-1}\right) = V_{in}$$

Here D_0 is a binary digit 1 or 0 and LSB and D_{n-1} is the MSB.

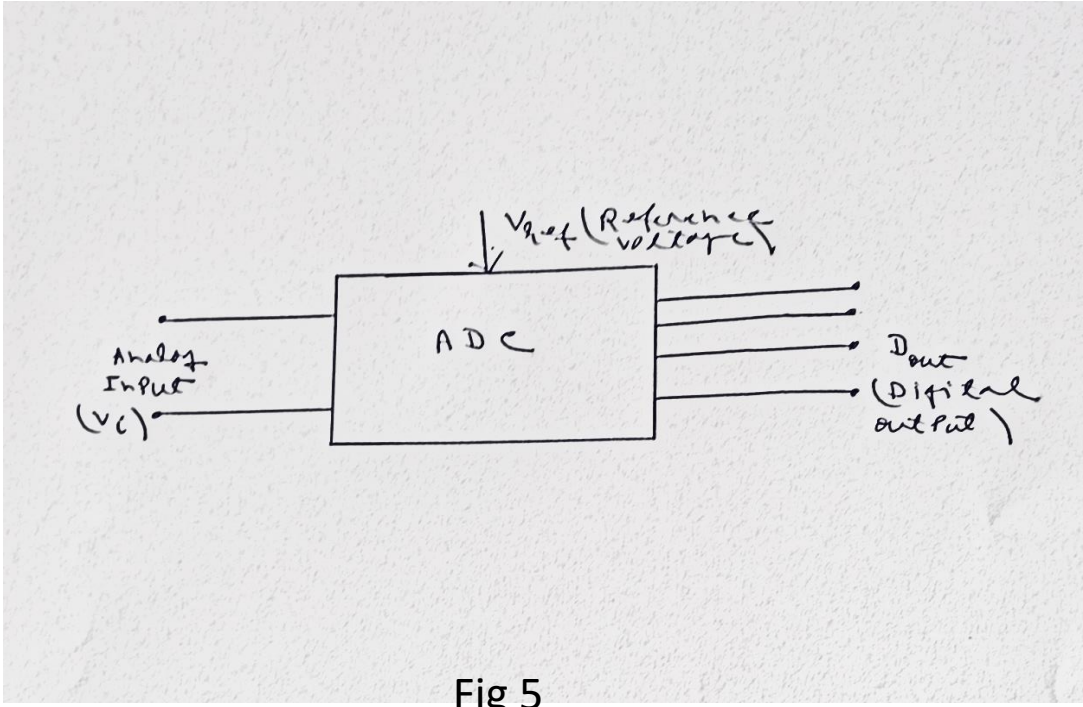

Fig 5

Here D_0 is a binary digit 1 or 0 and LSB bit and D_{n-1} is the MSB. The process of analog to digital conversion is also called quantization. This process is more complex and time consuming as compared to digital to analog conversion. Again in this process there is loss of some information which is called **quantization error** or **quantization noise**.

Successive Approximation Conversion(SAC):

In this method there are some advantages like it has much shorter conversion. Time than that other type. Again it has a fixed conversion time which does not depend on the value of the analog input.

It consists of a DAC , an output register, a comparator and control logic.

At first the bits of DAC are enabled one at a time starting with MSB. As each bit is enabled, the comparator produces an output that indicates whether the input voltage is greater than or less than the output of DAC is V_{ref} .

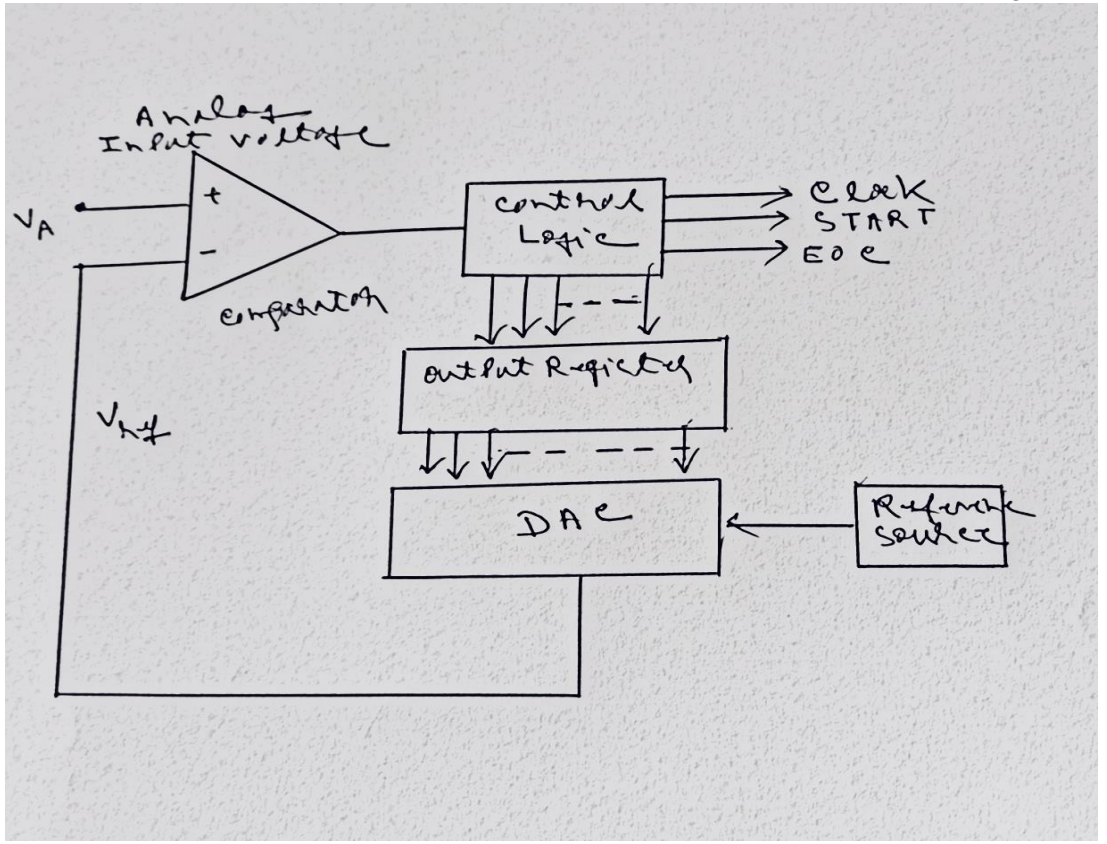

Fig 6

If the DAC output is greater than the analog input, the comparator output is LOW , which will cause the bit in the control register to reset. But if the DAC output is greater than the analog input, the comparator output is HIGH and the bit is retained in the control register. The system the MSB first, then the next significant bit and so on. After all the bit is one clock cycle, so total conversion time for a N-bit Successive Approximation (SA) type DAC will be N clock cycles.

$$Conversion\ Time(t_c) for\ SAC = N \times 1\ clock\ cycles$$

It means conversion time will be same and will not depend on the value of analog voltage V_A . This SA-DAC can give conversion speeds upto about 10^5 samples per second at good resolution.