Electronics
Lecture 6

(For Sixth Semester General Course)

Manoj Kr. Das

Associate Professor

Physics Department

J N College, Boko

Logic Gate:

A logic gate is an idealized model of computation or physical electronic device implementing a Boolean function, a logical operation performed in one or more binary inputs that produces a single binary output. The basic logic gates are OR, AND and NOT gates.

OR gate:

An OR gate has two or more inputs but a single output. The output of the OR gate is in the state 1 if one or more inputs assume the state 1. Where A and B are the two inputs and Y is the output of the OR gate.
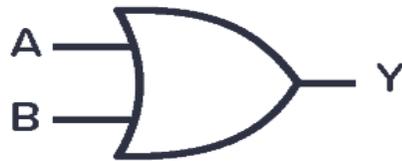

Fig 1

Input A	Input B	Output y
0	0	0
0	1	1
1	0	1
1	1	1

Table 1 . Truth Table of OR Gate

The *Table* 1 gives the truth table representing of two input OR gate, the 0 and 1 in the truth table represent the low or 0 volt and high or 5 volt
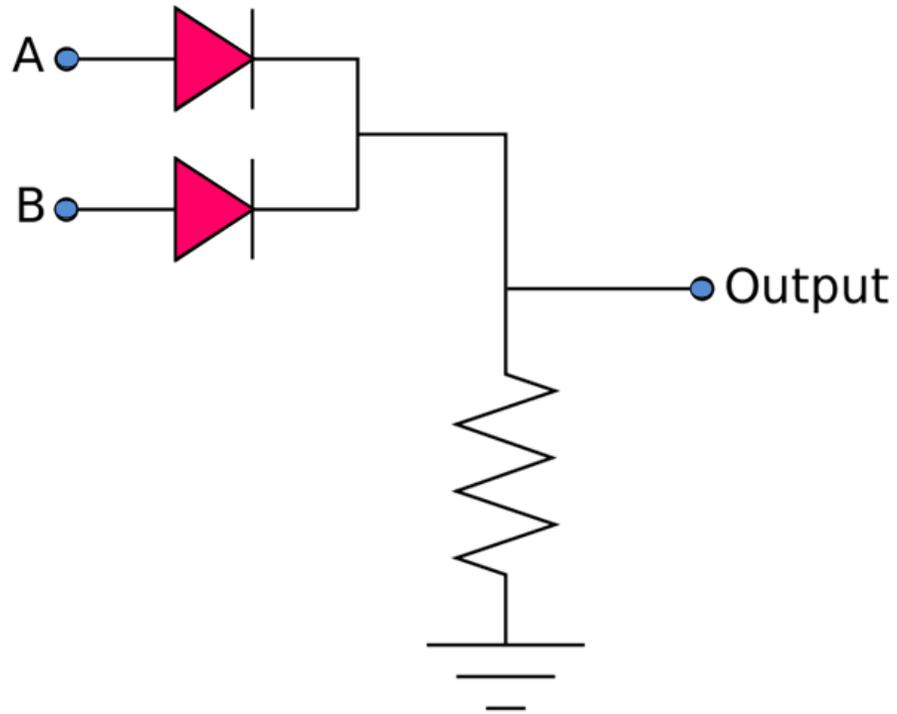
A

B

Output

Fig 2

Transistor
OR Gate

© www.petervis.com
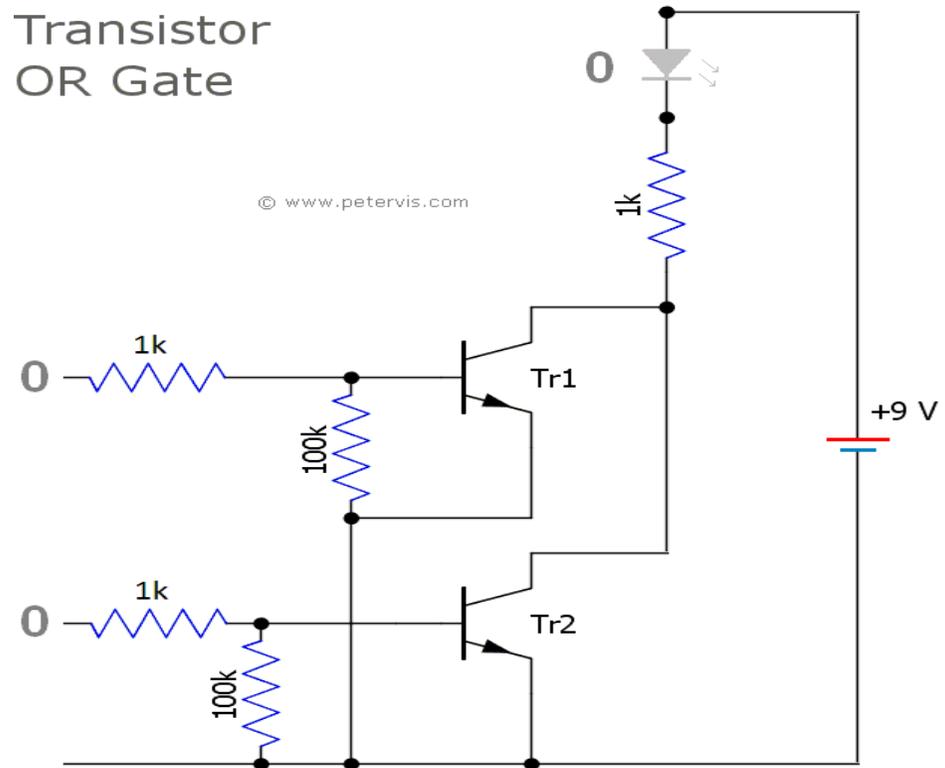
1k

0

1k

0

100k

Tr1

100k

Tr2

1k

0

+9 V

Fig 3

AND Gate:

An AND gate possesses two or more inputs and a single output. The output of an AND gate is in 1 if and only if all the inputs assume the state 1. Consequently an AND gate is also referred to as a coincidence circuit. The operation of an AND can be given in $Table$ 2. Here 0 volt and 5 volt represent the states 0 and 1 respectively
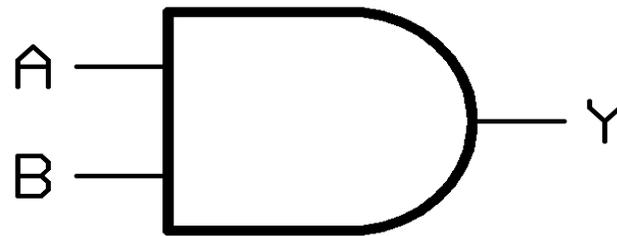
Fig 4

Input A	Input B	Output Y
0	0	0
0	1	0
1	0	0
1	1	1

Table 2: Truth Table of AND Gate

A diode logic configuration of two input AND gate for positive logic circuit. Here A and B are two inputs and y the output of AND gate.
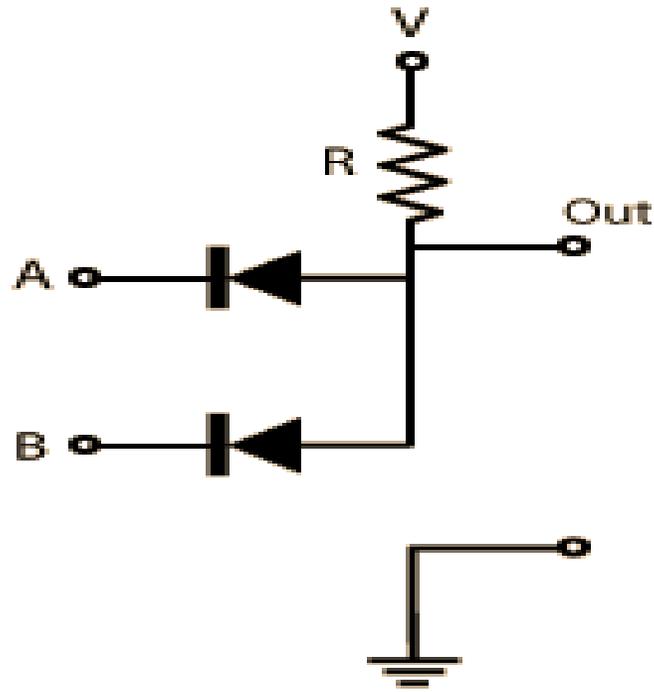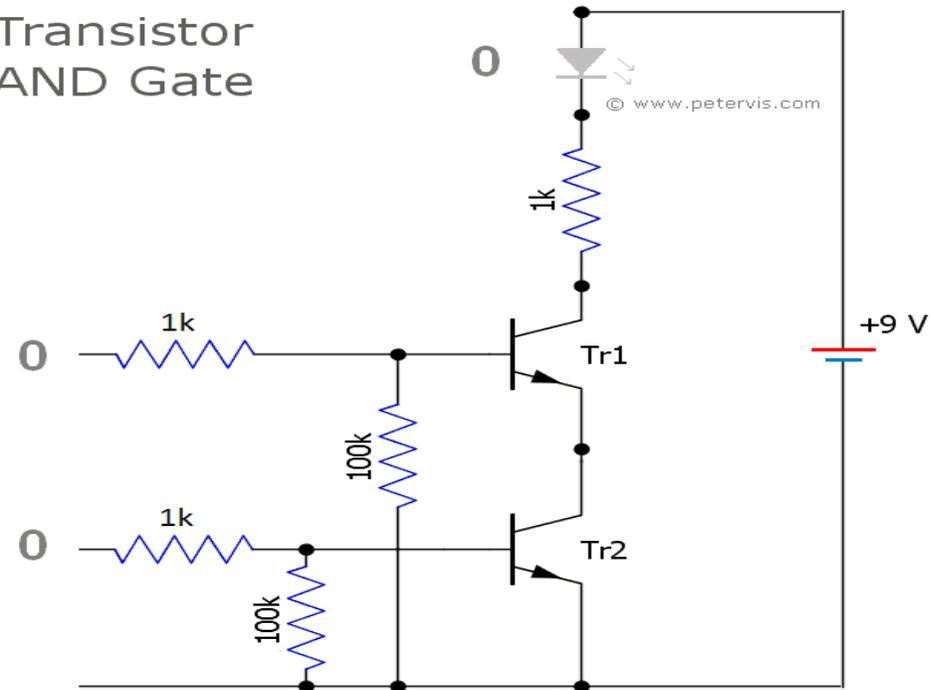

Fig 5

Transistor AND Gate

© www.petervis.com

Fig 6

NOT Gate:

The NOT circuit has single input and single output. The output of the NOT circuit is in the state 1 if and only if the input does not assume the state 1. The output of the circuit is therefore high when the input is low and vice versa. As the NOT circuit inverts the sense of the output with respect to the input it is also referred to as an inverter. The NOT operation is also known as negation.
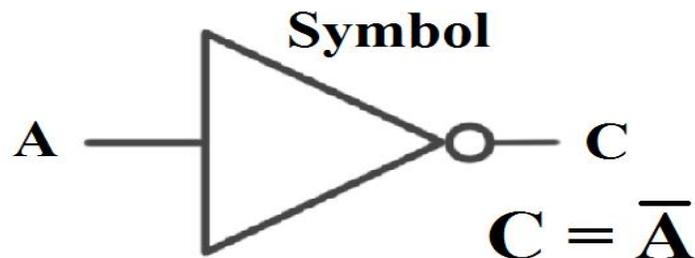
Symbol

$$C = \overline{A}$$

Fig 7

INPUT	OUTPUT
A	NOT A
0	1
1	0

Table 3: Truth Table of NOT Gate

A transistor circuit implementing an inverter as shown in figure. When the input voltage is low the transistor is cut off and the output voltage is $v_0 = V_{cc}$. Thus output is high. However if the input voltage is high the transistor saturates and the output voltage becomes low.
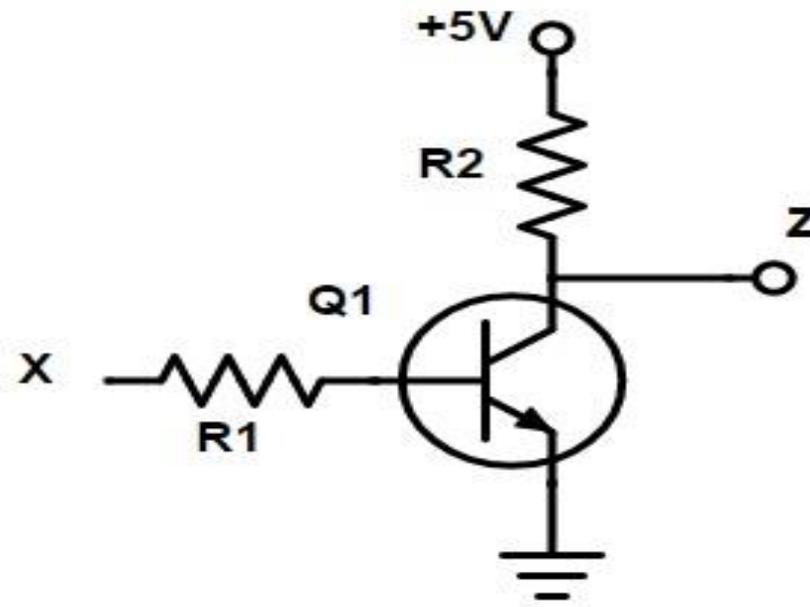

Fig 8

NOR Gate:

The logic circuit where a NOT gate follows an OR gate is termed as NOT-OR or NOR gate. NOT circuit can be constructed with transistor where OR gate can be constructed with diodes or transistors. Therefore NOR gate can be realised by diode-transistor logic
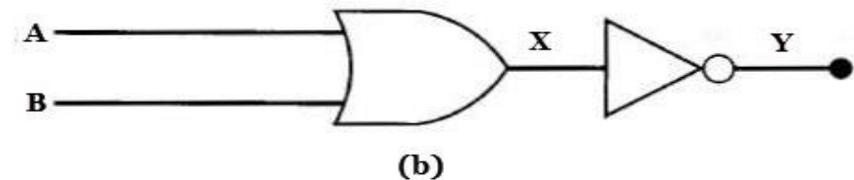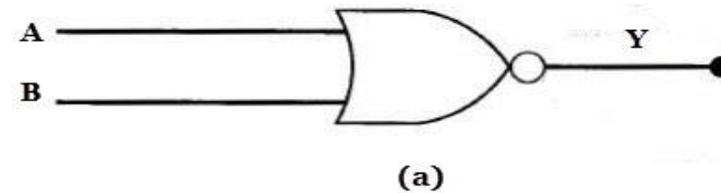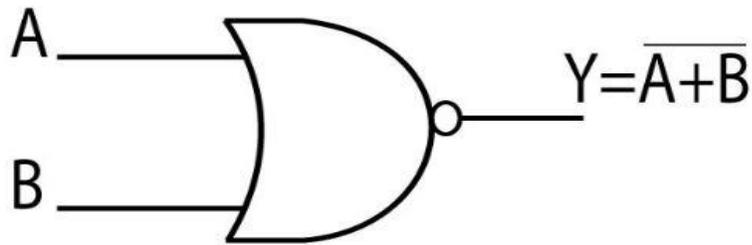

Fig 9

Input A	Input B	Output Y
0	0	1
0	1	0
1	0	0
1	1	0

Table 4: Truth Table of NOR Gate

The NOR gate is the basic gate in the resistor-transistor logic family produced by IC technology. It consist of only resistors and transistors.
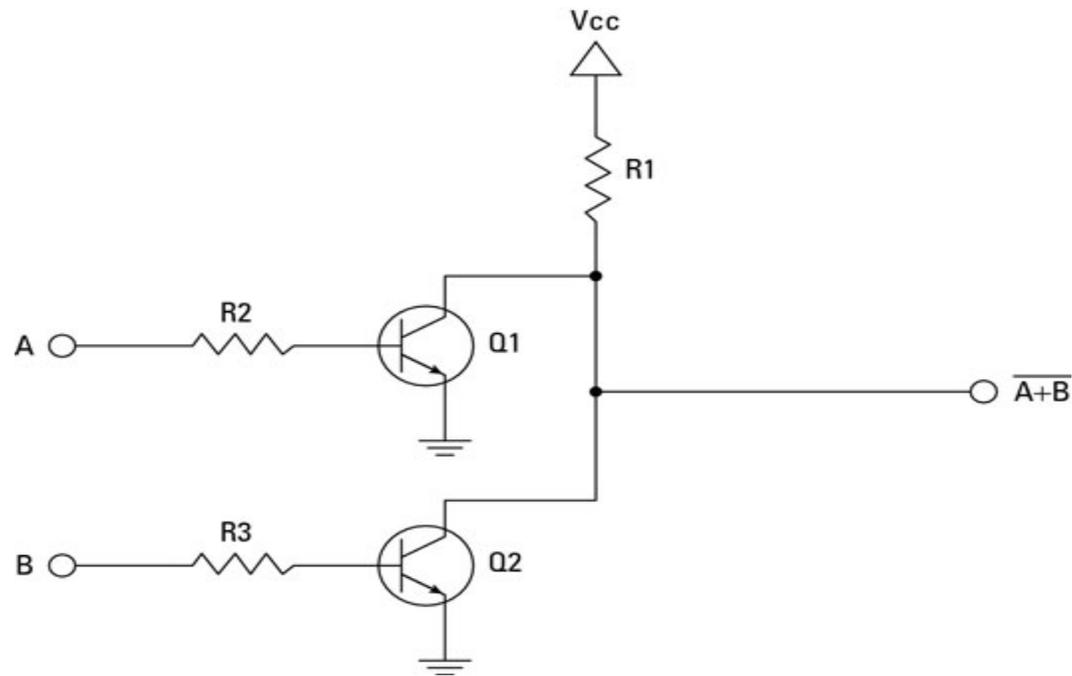

Fig 10

NAND Gate:

The logic circuit in which a NOT gate follows an AND gate is referred to as a NOT-AND or NAND gate. The Boolean expression characterising the NAND gate $Y = \overline{A.B}$. The NOT gates can be built with transistors and AND gates can be constructed with diode or transistors. Consequently NAND gates can be built with diode-transistor logic.
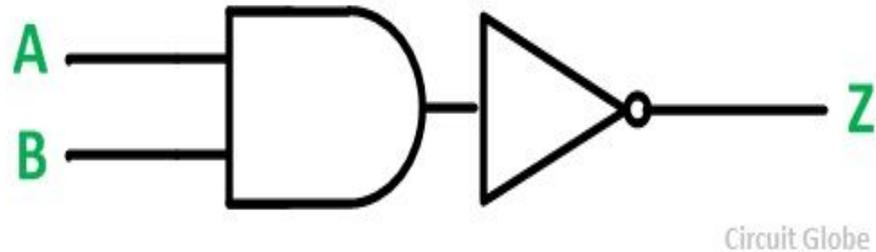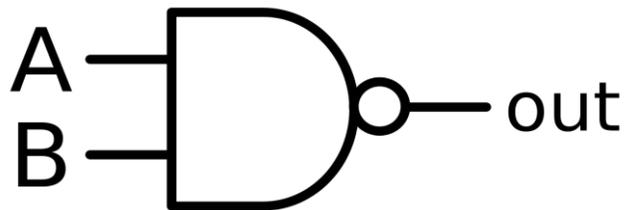

Fig 11

Input A	Input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

Fig 5: Truth Table of NAND Gate

The NAND gate is the basic gate in DTL or the TTL family by IC. A positive logic DTL NAND gate consists of the diode AND gate followed by a transistor NOT gate with some modifications. The output of the AND gate is coupled to the base of the transistor of the NOT circuit through two diodes in series.
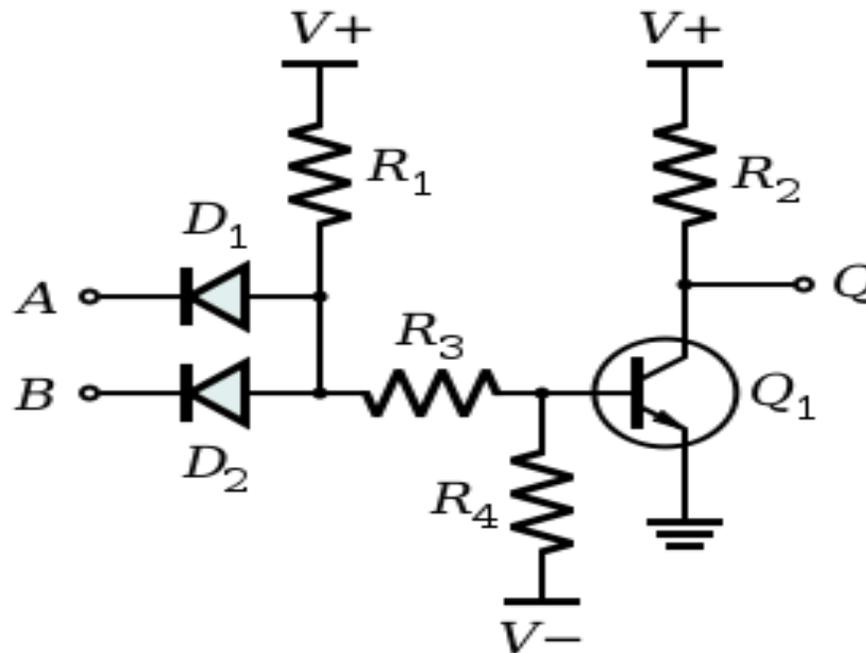

Fig 12

De Morgan's Theorem:

First Theorem: $\overline{A + B} = \bar{A}.\bar{B}$

Second Theorem: $\overline{A.B} = \bar{A} + \bar{B}$

Some Useful Laws:

(A)Communitive Law

$$A + B = B + A$$
$$A.B = B.A$$

(B)Associative Laws

$$A + (B + C) = (A + B) + C$$
$$A.(B.C) = (A.B).C$$

(C)Distributive Laws

$$A.(B + C) = A.B + A.C$$

The basic OR relation are
$$A + 0 = A$$
$$A + 1 = 1$$
$$A + A = A$$
$$A + \bar{A} = 1$$

The basic AND relations are

$$A.0 = 0$$
$$A.1 = A$$
$$A.A = A$$
$$A.\bar{A} = 0$$

(D)Absorptive Laws:

$$A + A.B = A$$
$$A.(A + B) = A$$

The Boolean Inequalities are

$$A(\bar{A} + B) = A.B$$

$$A + \bar{A}.B = A + B$$

$$A + B.C = (A + B).(A + C)$$

$$(\bar{A} + B).(A + C) = \bar{A}.C + A.B$$

$$(A + B).(B + C).(C + A) = A.B + B.C + C.A$$

$$\bar{A}.B.\bar{C} + \overline{A}.B.C + A.B\overline{.C} = B.(\bar{A} + \bar{C})$$

Thevinin's Theorem:

Any two terminal linear network connecting energy source (Generator) and impedance can be replaced with an equivalent circuit consisting of voltage source (E') in series with an impedance (Z')
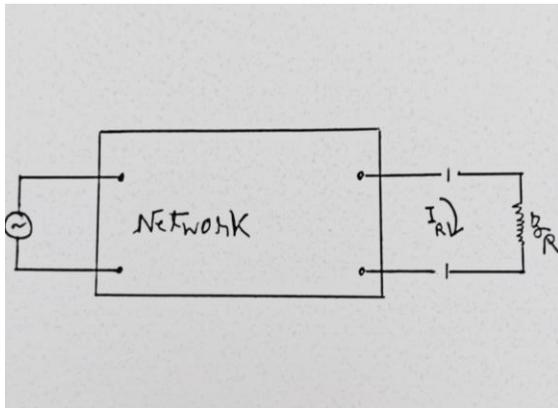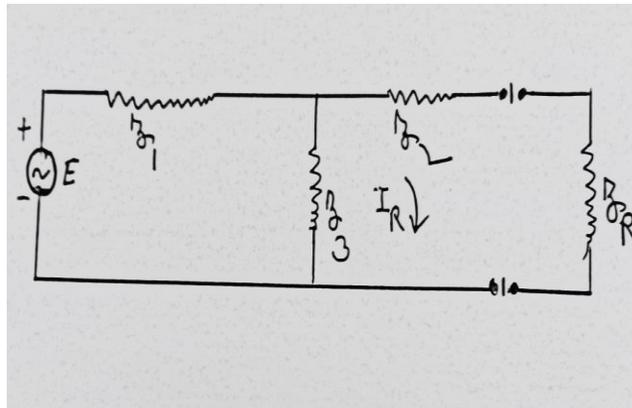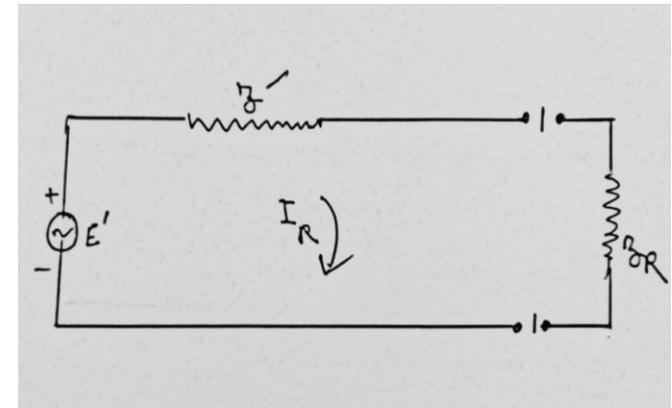

Fig 13

Fig 14

Fig 15

The value of E' is the open circuit voltage between the terminals of the network and Z' is the impedance measured between the terminals with all energy source eliminated(but not their impedance). In Fig 13, network represent by box between generator and terminal (1,1) may be replaced by T-section. Considering Fig 14, the mesh equation is

$$E = I_1(Z_1 + Z_3) - I_R Z_3$$

$$0 = -I_1 Z_3 + I_R(Z_2 + Z_3 + Z_R)$$

Then

$$I_1 = I_R \frac{Z_2 + Z_3 + Z_R}{Z_3}$$

And

$$I_R = \frac{E}{\dfrac{(Z_1 + Z_3)(Z_2 + Z_3 + Z_R)}{Z_3} - Z_3}$$

$$I_R = \frac{EZ_3}{Z_2(Z_1 + Z_3) + Z_1 + Z_3 + (Z_1 + Z_3)Z_R}$$

Dividing by $(Z_1 + Z_3)$

$$I_R = \frac{E\left(\dfrac{Z_3}{Z_1 + Z_3}\right)}{Z_2 + \dfrac{Z_1 Z_3}{Z_1 + Z_3} + Z_R}$$

Open voltage at (1,1) terminal is

$$E' = E \left(\frac{Z_3}{Z_1 + Z_3} \right)$$

And impedance of the network measured between (1,1) terminal with all generators emf short circuit is

$$Z' = Z_2 + \frac{Z_1 Z_3}{Z_1 + Z_3}$$

Therefore

$$I_R = \frac{E'}{Z' + Z_R}$$

This is the current equation. The theorem has therefore been proved for network containing one generator.

Norton's Theorem:

Any two terminal linear network containing energy source (Generator) and impedance can be replaced with an equivalent circuit consisting of a current source (I') in parallel with an admittance (Y').
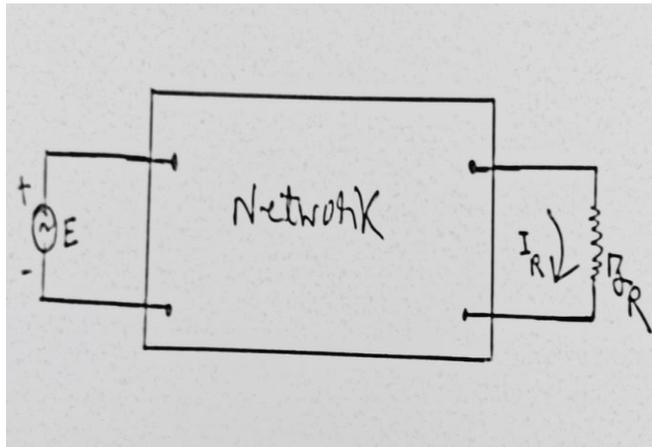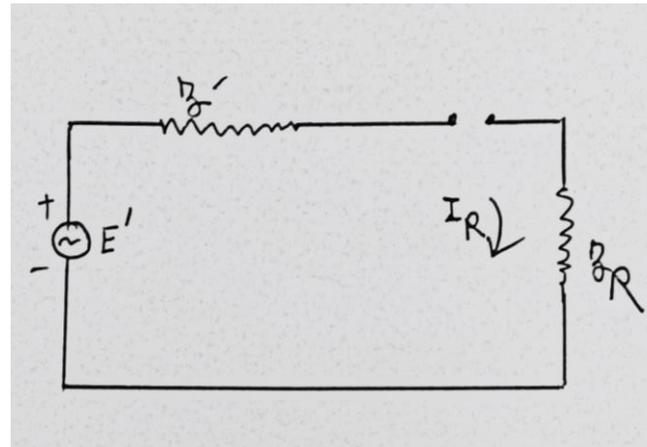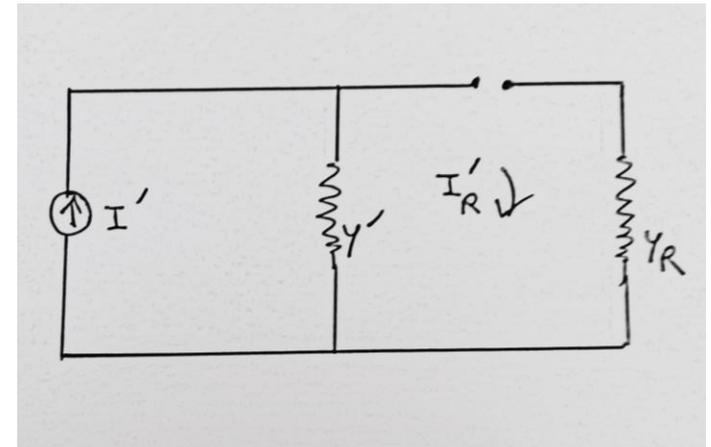

Fig 16

Fig 17

Fig 18

The value of I' is the short circuit current between the terminals of the network and Y' is the admittance measured between terminals of the network with all energy sources eliminated (but not their admittance).

This theorem produces an equivalent circuit that is as useful for parallel connected active network as the voltage source equivalent is for series connected active network. This theorem may be proved by considering any network reduced by Thevinin's Theorem. Here

$$I_R = \frac{E'}{Z' + Z_R} = E'Y'\left(\frac{Y_R}{Y' + Y_R}\right)$$

Now considering circuit as shown in Fig 18 where a constant current generator of I' supplies current to a parallel network of two admittances Y' and Y_R. By use of appropriate current division factor the current I_R' in the load admittance Y_R may be written as

$$I_R' = I' \left(\frac{Y_R}{Y' + Y_R} \right)$$

The load current I_R' may be made equal to that of I_R in circuit.

If $I' = E'Y' = \frac{E'}{Z'}$, then the circuit as shown in Fig 18 and Fig 19 are equivalent. The current I' may be recognized as that circuit current of the Thevinin's equivalent network.

If the current output of the current generator I' , the current source network of Fig 19 is shown equivalent to Thevenin's circuit and to original network.

Interchange of voltage and current sources by means of Thevinin's and Norton's Theorem produces a powerful method of circuit analysis. In such conversion it should be noted that a voltage is removed from a circuit by short circuiting its emf whereas where a current source is removed by opening its circuit.